Radio Shack®

Service Manual

26-1143

TRS-80®

Model I Double-Density Adapter Kit

Catalog Number 26-1143

CUSTOM MANUFACTURED IN U.S.A. FOR RADIO SHACK, A DIVISION OF TANDY CORPORATION

TRS-80® Model I
Double-Density Disk System
Manual

CONTENTS

Introduction

The Double-Density Disk System for the TRS-80 Model I allows more storage on a 5 1/4 inch diskette than is available on a single-density diskette. An 80% increase in disk-storage capability is available using 35 tracks and more than double the capacity if 40 tracks is used.

To use this capability, you must have a Double-Density operating system and a hardware modification. The new operating system is on a diskette and the description of its use is found in the Double-Density Disk System Owner's Manual (26-1143). The hardware modification is an Adapter Board that must be installed by a qualified Radio Shack Service Technician.

This Adapter Board allows the continued use of single-density diskettes with a single-density operating system as well as the enhanced double-density system.

Model I with double-density is capable of reading Model III data diskettes, but this feature is not supported in the Double-Density Operating System (DDOS). The operating systems are not compatible because of addressing differences. Therefore, the software does not support full compatibility. Shugart disk drives will NOT support a 40 track operation. The disk drives that have a serial number that is followed by a (-1) are manufactured by Tandon or Texas Peripherals and are certified for double-density and can be CONFIGured to 40 tracks.

The design objective was to make the double-density adapter fully compatible with the Western Digital 1771 socket inside the Model I expansion interface. This is an easy plug-in installation without trace cuts or jumpers. In addition, a side select line is available on the adapter board for future enhancements. This modification, however, would require changes to the expansion interface.

1/ Functional Specifications

The TRS-80 Model I Double-Density Adapter Board is an optional "add-on" board for the Model I which provides a double-density controller for the 5 1/4 inch floppy disk drives. This board can support both single and double-density operation.
This modification, along with the software required for operation, allows the transfer of Model I single-density files to double-density format.

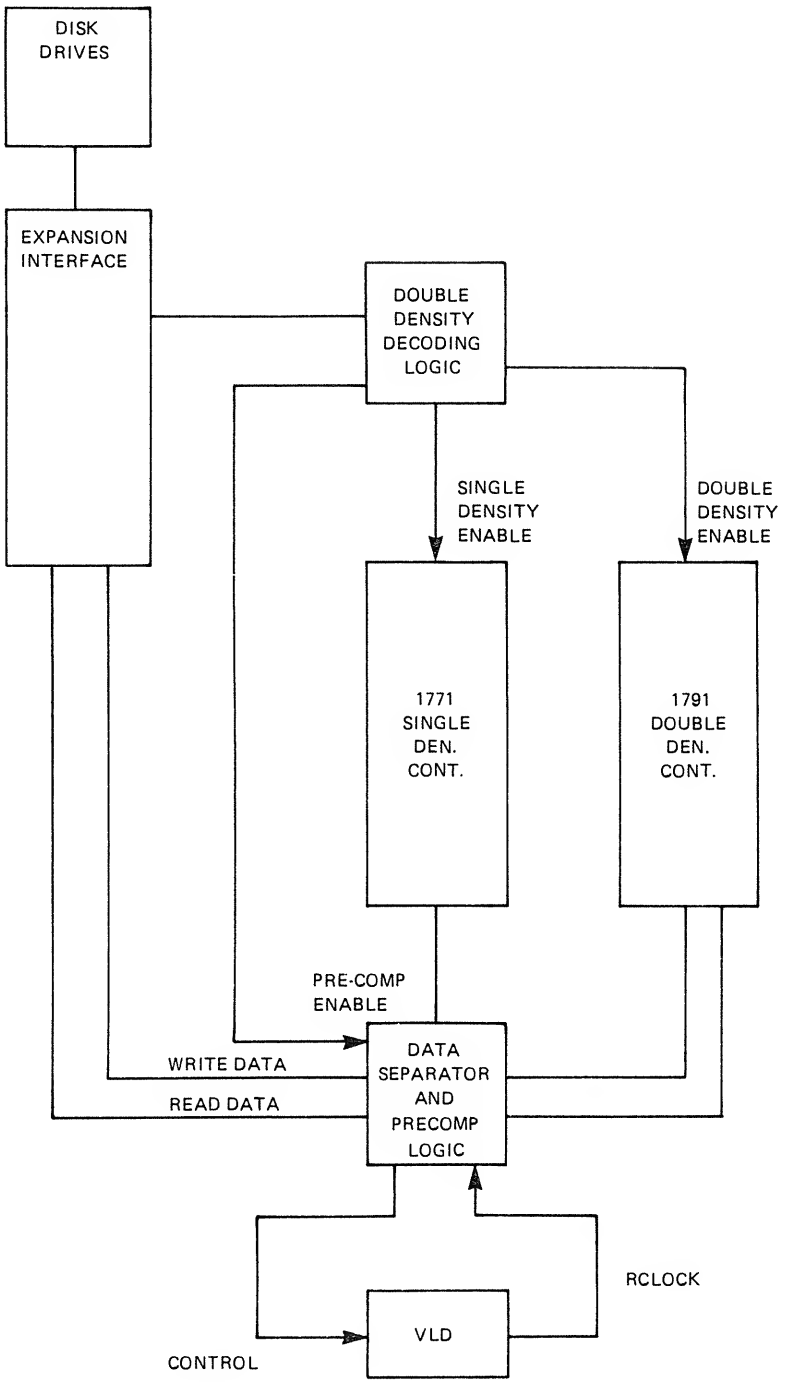
Write precompensation is provided and is software controlled for any desired track. System software automatically enables precompensation for all tracks greater than 21. The amount of write precompensation is hardware adjustable on the Adapter Board from 0ns to 500ns. The adapter boards are adjusted at the factory for a nominal rate of 200ns.

The data-clock recovery circuit incorporates a phase-locked loop system for state-of-the-art reliability.

Upon reset or power-up, the Adapter Board is configured for side 0, no precompensation, and single-density. If a single-density operating system is used, the Model I will not change from that density. If a double-density operating system is used, the Model I will reconfigure the Adapter Board to operate in double-density.

In the double-density operation, data transfers are synchronized to the CPU by polling the FDC for a data request before the operation begins. If good status is not received after a specified length of time, the operation is aborted and control is returned to the calling program.

2/ Block Diagram



3/ Installation

Before installation of the Model I Double-Density Adapter, verify the proper operation of the Expansion Interface using a memory test, FORMAT, and BACKUP for single-density. This installation should only be attempted after the Expansion Interface is proved to be functioning properly.

1. Remove the Power Supply Cover on the Expansion Interface and remove and disconnect the power supplies.

2. Turn the E. I. upside down and remove the six screws that hold the case together. Remove the bottom cover. The screws are of different lengths (remember which screws went where), and must be used to reinstall the Bottom Cover.

3. Locate the WD 1771 FDC chip. It is the only 40 pin chip in the E. I. It is Z34 on revisions A and C boards and Z42 on the revision D board. Carefully remove this chip. After removing the chip, carefully check and straighten any bent pins, and insert the chip in the socket for U3 on the new DDA board.

4. The Adapter Board is mounted (installed) in the socket on the Expansion Interface board where the WD 1771 FDC chip was removed. There are extension pins below the adapter circuit board for this purpose. Be certain that the FDC chip is facing the same direction as it was on the E. I. board (#1 pin is over #1 pin, etc). Carefully set the Adapter Board OVER the socket (in the E. I.) so that the ends marked for pin #1 are aligned and that the pins will go in the socket. Then press evenly on the board to firmly seat the pins in the socket.

5. It is unlikely that you will need to bend any capacitors to seat the adapter board. If you must, be sure to not cause a short or break any leads.

6. Lay the piece of foam, included with the unit over the Adapter Board. Carefully reinstall the Bottom Cover. Then turn the E. I. back over and reconnect the power supplies and replace the Power Supply Cover.

7. Apply power to the unit and boot either the single-density or the double-density version of TRSDOS. Do not try to boot Model III TRSDOS. If TRSDOS will not boot, first attempt steps 1 and 2

of the alignment procedure (see "Alignment") before going on to the "Troubleshooting" section of this manual.

8. Go to the "Alignment" section of this manual.

4/ Alignment Instructions

1. TP9 is the Frequency control point for the Voltage Control Oscillator circuit (U13). It should be adjusted when instructions are not being executed by the Floppy Disk Controller (idle state). Adjust R7 so that the level of 1.4 volts is obtained with reference to ground.

2. The VCO free-running frequency must also be adjusted in an idle state and in single-density mode. The measurement at TP5 should be adjusted as close as possible to 125 kHz but on the low side (i.e. 124.99 kHz). The adjustment is made using R11.

3. Write precompensation must be adjusted while executing disk writes and is measured at TP6. Boot TRSDOS (either version) and format a blank diskette. While it is formatting, adjust R2 so that the pulse width on TP6 is 2ØØ ns in duration.

When a version of Tandy Drive Controller (TDC) is available, execute continuous track writes. This will be much easier than trying to catch the pulse during the FORMAT operation.

TEST POINTS

TP#	NAME	WHAT YOU SHOULD SEE
1	CLK	1 mhz clock from E. I.
2	DDEN*	Ø for double-density 1 for single-density
4	IP*	Index pulse from disk drive
5	RCLK	125 kHz in idle condition (R11) (drive not running)
6	Precomp	2ØØ nsec duration pulse when enabled and writing (R2)

7	PREN	Ø for No Precomp 1 for Precomp enable
8	Ground	Ground
9	FDC Bias	1.4 VDC in idle position (R7)

ADJUSTMENT POTENTIOMETERS

R2 Precomp Adjust (TP6)

R7 Bias Adjust (TP9)

R11 Free Run Adjust (TP5)

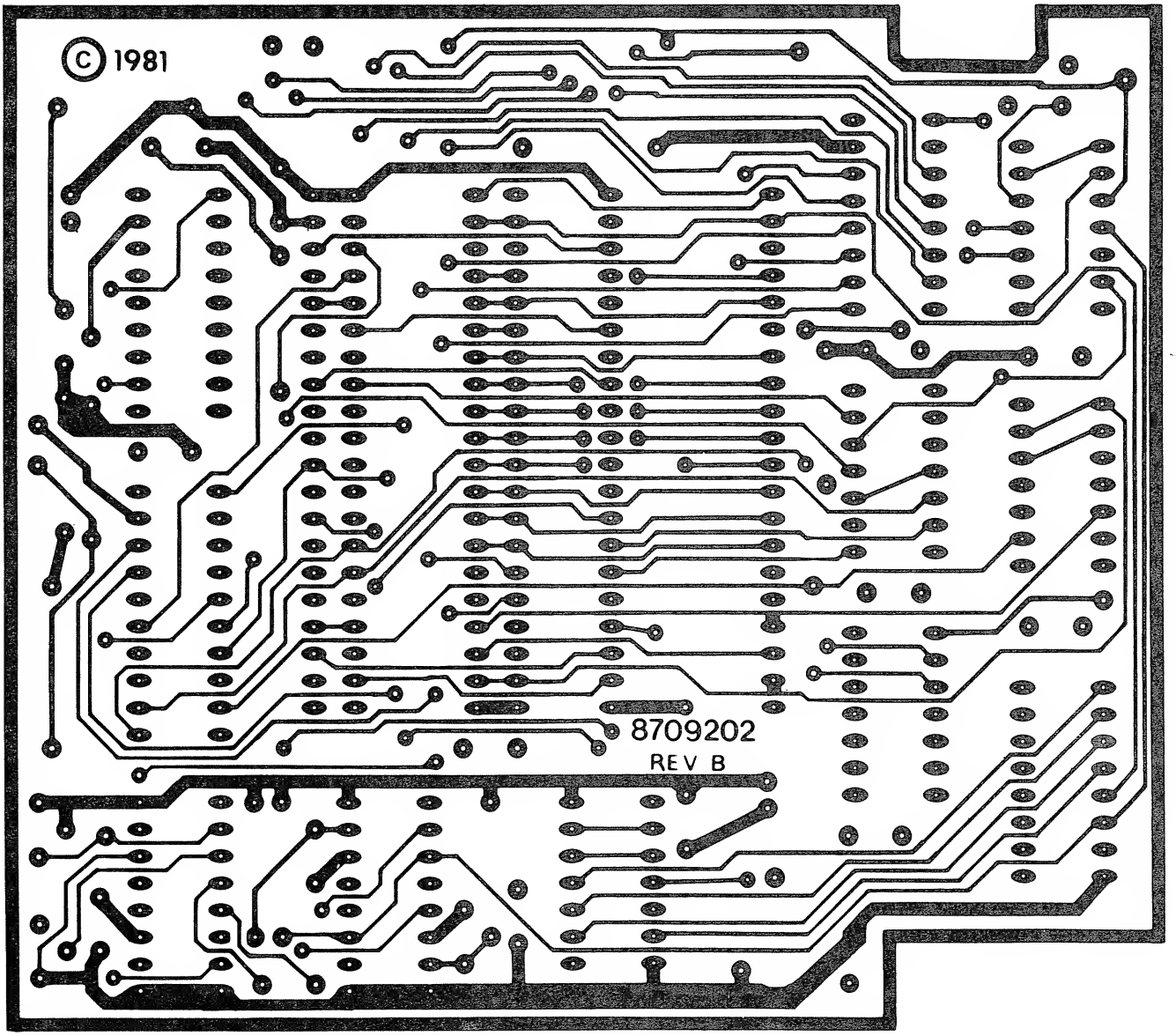
5/ Troubleshooting

SYMPTOM	POSSIBLE PROBLEM(S)
Powers-On to Ready >	a,b,c,d,e, or f
Powers-On with garbage on Screen (Drive does not turn-on after RESET)	e,f,h,i, or k
Powers on with garbage on screen (Drive turns-on after RESET)	a - f, h, j, k, or l
All drives stay turned-on	g or k
Starts to boot DDOS, but hangs up at 'LOADING TRSDOS' message	j, l, or m
Will not FORMAT or write (Single-density)	d or l
Will not FORMAT or write (Double-density)	l, m or o

Explanation of problems

a. Double-Density Adapter not seated properly
b. Bent pins on header strip
c. Bent pins on WD1771 (U3)
d. Bad WD1771 (U3)
e. E. I. power supply not plugged in or not turned-on
f. Bad cable (CPU to E. I.)
g. Cable upside down (E. I. to Disk Drive(s))
h. If buffered cable, is it plugged in backwards?
i. Disk Drive(s) turned off?
j. Bad Operating System diskette
k. Bad cable (E. I. to Disk Drive(s))
l. Incorrect adjustments on board
m. Bad WD1791 (U4)

6/ Printed Circuit Board(solder side)



U3 1771

U2 LS157

U4 1791

U6 WD1691

U5 WD2143

U10 LS138

U11 LS10

U12 LS123

U13 74LS828

U1 LS74

U6 LS74

U7 08

U8 04

U9 04

1771 SOCKET HEADER

DRAFT | DATE | TITLE: DOUBLE DENSITY ADAPTER

CHECK | DATE

DESIGN | DATE

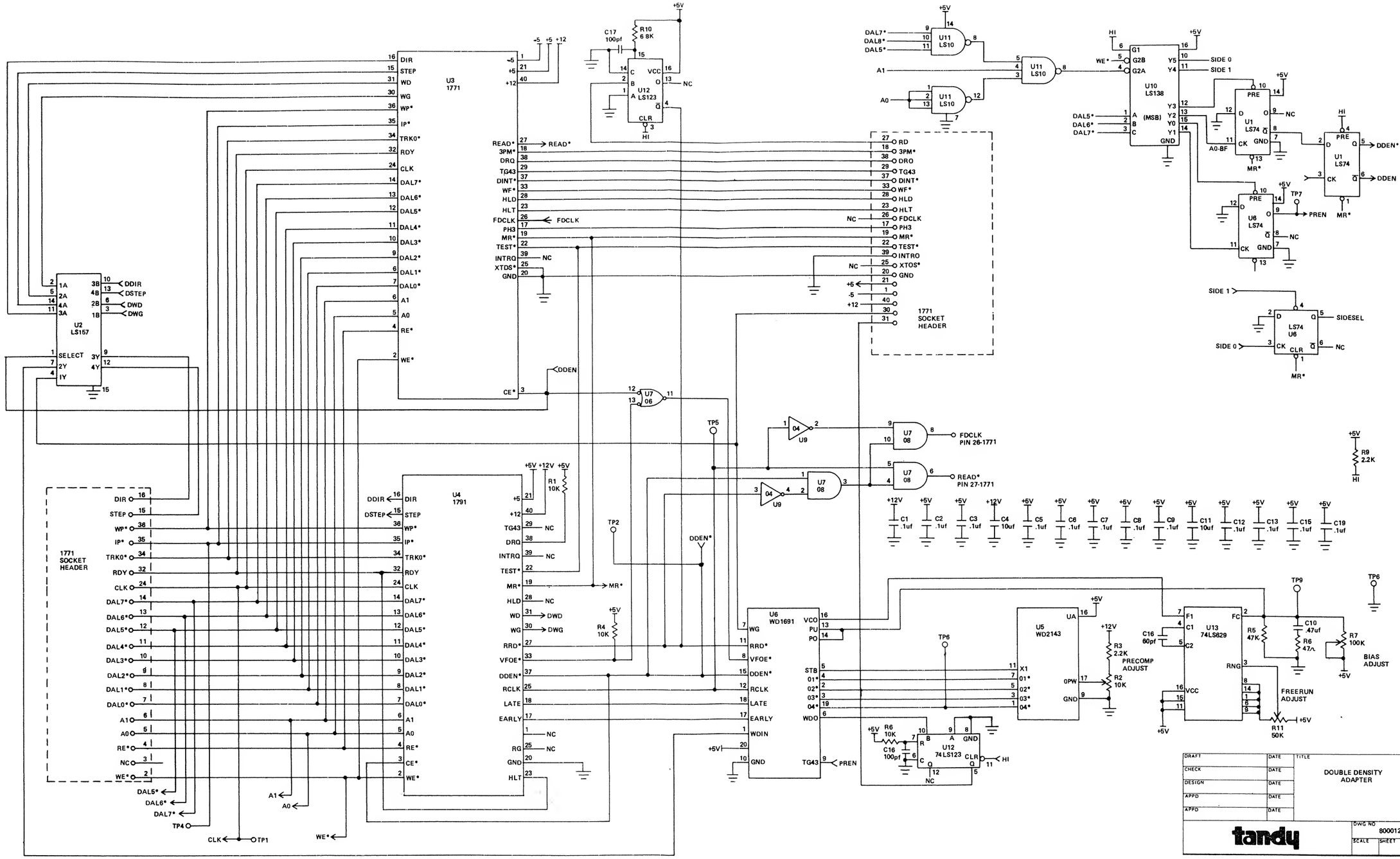
APPD | DATE

APPD | DATE

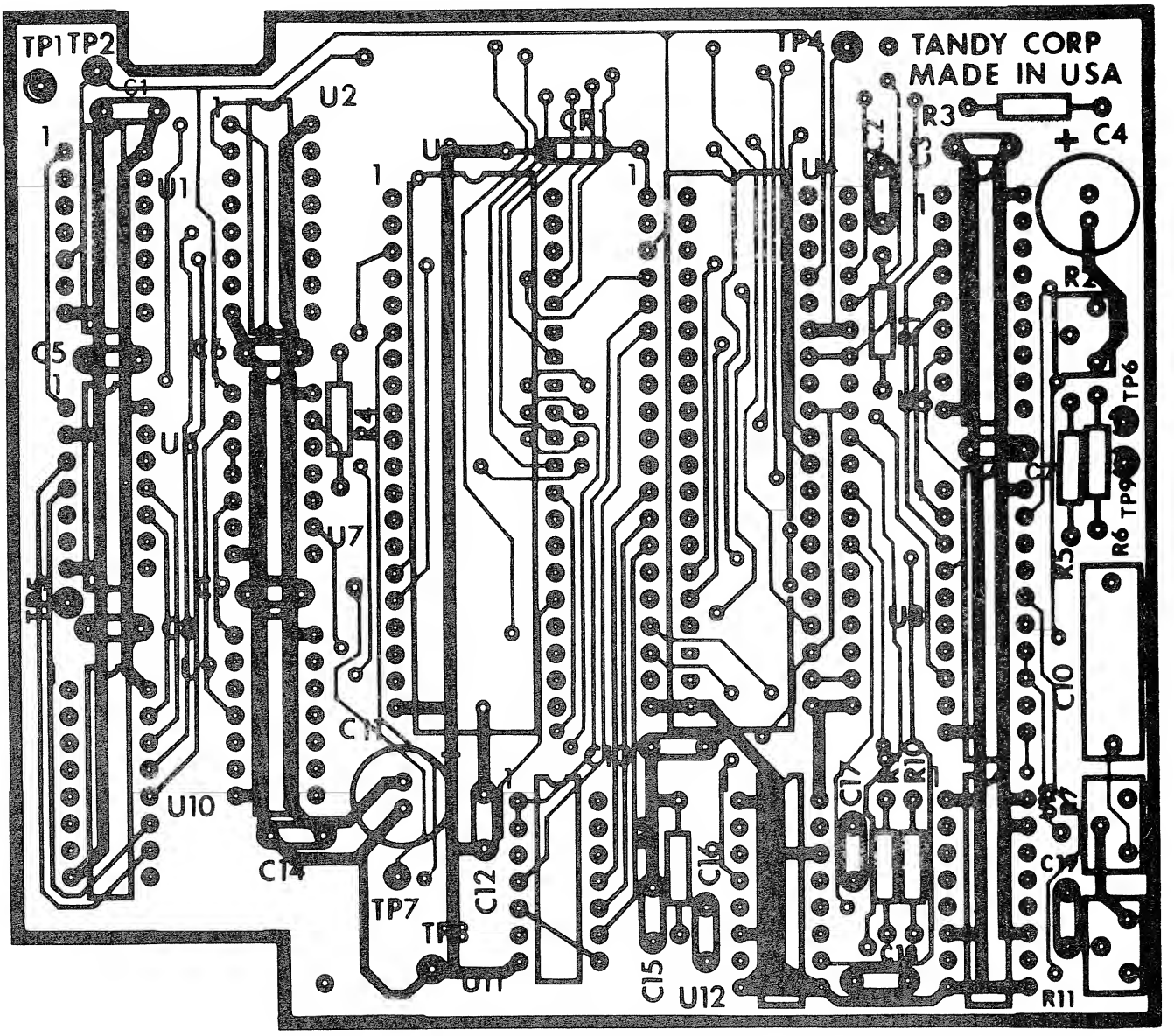
tandy

DWG NO 8000126 | SIZE

SCALE | SHEET 1 OF 1


U3 1771
U2 LS157
U4 1791
U6 WD1691
U5 WD2143
U13 74LS629
U12 LS123
U10 LS138
U11 LS10
U7 08
U9 04
U1 LS74
U8 LS74
U6 LS74
1771 SOCKET HEADER
DIR
STEP
WD
WG
WP*
IP*
TRK0*
RDY
CLK
DAL7*
DAL6*
DAL5*
DAL4*
DAL3*
DAL2*
DAL1*
DAL0*
A1
A0
RE*
WE*
CE*
DDIR
DSTEP
DWD
DWG
SELECT
READ*
FDCLK
DDEN
MR*
PREN
WDIN
SIDE 0
SIDE 1
SIDESEL
DDEN*
BIAS ADJUST
PRECOMP ADJUST
FREERUN ADJUST
DOUBLE DENSITY ADAPTER
tandy
DWG NO 8000126

(Component side and components)



7/ Schematic

8/ Parts List

SYMBOL	DESCRIPTION	MANUFACTURER'S PART NUMBER	RADIO SHACK PART NUMBER
	RESISTOR/TRIM POT		
R1, R4, and R8	Resistor, 10K ohm, 1/4 watt, 5%	820-7310	AN0281EEC
R2	Trim Pot, 10K ohm, .151 watt	827-9310	AP7167
R9, R3	Resistor, 2.2K ohm, 1/4 watt,5%	820-7222	AN0216EEC
R5	Resistor, 47K ohm, 1/4 watt, 5%	820-7347	AN0340EEC
R6	Resistor, 47 ohm, 1/4 watt, 5%	820-7047	AN0099EEC
R7	Trim Pot, 100K ohm, .151 watt	827-9410	AP0834
R10	Resistor, 6.8K ohm, 1/4 watt, 5%	820-7268	AN2262EEC
R11	Trim Pot, 50K ohm, .151 watt	827-9350	AN7168
	CAPACITORS		
C1-C3, C5-C9, C12-C15, and C19	1 mfd, 50 volt, monolithic, radial	838-4104	ACC104QJAP
C4, C11	33 mfd, 16 v, electrolytic, radial	832-6331	ACC336QDAP
C10	47 mfd, 100 volt, 10% polyester	835-4475	ACC474KLGP
C16,C17	100 pfd, 50 volt, ceramic disk	830-1104	ACC101QJCP
C18	75 pfd, 50 volt, ceramic disk	830-0754	ACC750QJCP
	INTEGRATED CIRCUITS		
U1, U6	74LS74 Flip Flop	802-0074	AMX3558
U2	74LS157 Multiplexer	802-0157	AMX3563
U3	WD1771 (removed from EI to multiplexer)	802-5771	
U4	WD1791B-02 Floppy Disk Formatter	804-5791	AXX3014
U5	WD2143-01 4-Phase Clock	804-0143	AMX4472
U7	74LS08 Quad (2 input) And gate	802-0008	AMX3698
U8	WD1691 Floppy support logic	804-1691	AMX4471
U9	74LS04 Hex Inverter	802-0004	AMX3552
U10	74LS138 3 to 8 Decoder	802-0138	AMX4583
U11	74LS10 Triple input Nand gate	802-0010	AMX3898
U12	74LS123 Multivibrator (one shot)	802-0123	AMX3803
U13	74LS629 VCO	802-0629	AMX4663

SYMBOL	DESCRIPTION	MANUFACTURER'S PART NUMBER	RADIO SHACK PART NUMBER
	MISCELLANEOUS		
	Printed Circuit Board (Rev. B)	870-9202	NST
	Staking Pins	852-9014	AHB9682
U3	Socket 40-Pin DIP	850-9002	AJ6580
U4	Socket 20-Pin SIP	850-9013	AJ7125
U5	Socket 18-Pin DIP	850-9006	AJ6701
U8	Socket 20-Pin DIP	850-9009	AJ6760
	Header 20-Pos SIP with spacer	851-9132	AJ7126

9/ Theory Of Operation

A. CONTROL AND DATA BUFFERING

The Double-Density Adapter Board is a memory mapped device that uses the same decoding logic as the single-density system on the Model I. (For more information on the decoding logic, see decoding logic section of the Expansion Interface Service Manual). Control lines, such as DDEN* (double-density enable), PREN (precompensation enable), and SIDESEL (side select), are latched using a one of 8 decoder, U10 (74LS138), and U1, U6 (flip flops). The three high order bits (DAL5* - DAL7*) of the sector write register (37EEH) are used to control the decoder.

In single-density operation, the WD1771 Floppy Disk Controller is selected (using DDEN as the select). For double-density operation, the WD1791 FDC is used. The Double-Density Adapter Board includes both of these FDC's. The single-density FDC (WD1771) is moved from the Expansion Interface and the double-density FDC (WD1791) is a new part.

A WR* strobe in the address range 37ECH - 37EFH is decoded on the expansion interface as a write to the FDC. A1 must be high and A0 must be low to enable the decoder (U10) at the active low at G2A. The decoded address is 37EEH. In addition, if all the data lines DAL5*-DAL7* are high (this means a zero due to inverted logic) G2A will not go low. This prevents changing the state of the control lines on a normal write to the sector register. The following table illustrates the data used for each function:

DATA	FUNCTION
40-5F	Select side 0
60-7F	Select side 1
80-9F	Set double-density mode
A0-BF	Set single-density mode
C0-DF	Disable precomp
E0-FF	Enable precomp

Note that only one function may be toggled at a time. (i.e. one could not enable double-density and precompensation in one write to the sector register.) After selecting a control function, the data that was previously in the sector register will have been destroyed and should be rewritten if necessary.

B. RESET and CONTROL LATCHES

Upon RESET, the LS74 flip-flops for side select and precompensation enable are cleared. This mode sets side 0 and no precompensation. The two LS74's for the DDEN* are also cleared. However, upon the clock (1 MHz) from the Expansion Interface, the not Q output of the first flip-flop will be clocked as a high to the output of the second half of U1. The high at this output will cause the adapter to power-up in single-density.

Since both controllers share the data bus and other signals, they are selected and deselected using one signal, DDEN*.

C. WRITE PRECOMPENSATION and CLOCK RECOVERY CIRCUIT

All data transfers from disk, regardless of mode, use an external data separater/clock recovery circuit. This will provide more reliable data transfer than the unmodified Expansion Interface. U8 (WD1691), U5 (WD2143), and U13 (74LS629), along with a few passive components, comprise the write precompensation and read clock recovery logic. The WD1691 is a LSI device which minimizes the external logic required to interface the 1791 FDC chip to a disk drive. The use of an external VCO allows adjustment to keep the RCLK signal synchronous with the read data for the drive. Write precompensation control signals are also provided by the WD1691 to interface directly to the WD2143 clock generator. The read clock recovery section of the WD1691 has five inputs: DDEN*, VCO, RRD*, WG, and VFOE*/WF; and three outputs: PU, PD*, and RCLK. The inputs VFOE*/WF and WG when both low enable the clock recovery logic. When WG is high, a write operation is in progress and the clock recovery circuits are disabled regardless of the state of any other inputs.

The write precompensation section of the WD1691 was designed to be used with the WD2143 clock generator. Write precompensation is not used in the single-density mode and the signal DDEN* when high indicates this condition. In double-density mode (DDEN* = 0), the signals EARLY and LATE are used to select a phase input (01*-04*) on the leading edge of WDIN. The STB line is latched high when this occurs, causing the WD2143 to start its pulse generation. 02* is used as the write data pulse on nominal (EARLY = LATE = 0), 01* is used for the EARLY = 1, and 03* is used for the LATE = 1.

The leading edge of 04* resets the STB line in anticipation of th next write data pulse. When TG43 = 0 or DDEN* = 1, precompensation is disabled and any transitions on the WDIN line will appear on the WDOUT line.

When VFOE*/WF and WG are low, the clock recovery circuits are enabled. When the RRD* line goes low, the PU or PD* signals will become active. If the RRD* line has made its transition in the beginning of the RCLK window, PU will go from a high impedance state to a logic 1. This will cause the VCO to increase in frequency. If the RDD* line has made its transition at the end o: the RCLK window, PU will remain in the high impedance state while PD* will go to a logic 0. This will cause the VCO to decrease in frequency. When the leading edge of RRD* occurs in the middle of the RCLK window, both PU and PD* will remain in the high impedanc state, indicating that no adjustment of the VCO frequency is required. By tying PU and PD* together, an adjustment signal is created which will be forced low for a decrease in VCO frequency and forced high for an increase in VCO frequency. To speed up rise times and stabilize the output voltage, a resistor divider using R5, R6, and R7 (potentiometer) are used to adjust the tri-state level to approximately 1.4 v. This adjustment results in a worst case voltage swing of plus or minus 1v, which is acceptable for the frequency control input of the VCO (U13). The signal derived from the combination of PU and PD* will eventually correct the VCO input to exactly the same frequency multiple as the RRD* signal. The leading edge of the RRD* signal will then occur in the exact center of the RCLK window, an ideal condition for the WD1791 internal recovery circuits.

D. EXTERNAL DATA SEPARATION IN SINGLE DENSITY

In single-density mode, there is a separate clock bit for every data bit. This is not true in double-density. Therefore, external logic is required to interface the WD1691 Floppy Support Logic to the WD1771 Floppy Disk Controller. The purpose of this logic is to separate the clock and data bits in the data stream into two signals. This is done using one inverter (U9) and two AND gates (U7). This logic is also enabled using DDEN* and RRD* to detect single-density mode, and activity on the data line. On the rising edge of RCLK, the data bit is being decoded, and on the falling edge the clock pulse is decoded.

Two one-shots (sections of U12, 74LS123) are used to insure that the read and write data pulses are the necessary duration, from

about 300 to 450 nsec. Also, the VFO enable signal to the WD1691 is held active when in single- density.

E. FLOPPY DISK CONTROLLERS

The WD1771 is a single-density ONLY floppy disk formatter/controller. A detailed description of this device is given in the Expansion Interface Service Manual.

The WD1791 is an MOS LSI device which performs both the functions of a single and double-density floppy disk formatter/controller in a single chip. The 1791 is also used on the Model II FDC/Printer Interface board. The Model II Reference Manual contains a good presentation of the 1791 FDC chip as well as a discussion on write precompensation.

Both controllers share a common data bus and control lines, therefore, they are switched using DDEN. The following RAM addresses are assigned to the internal registers of the 1771/1791 FDC chips.

RAM ADDRESS	FUNCTION
37ECH	Command/Status Register
37EDH	Track Register
37EEH	Sector Register
37EFH	Data Register

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